REMARKS

Claims 1-7 remain present in this application.

The specification has been amended. Reconsideration of the application, as amended, is respectfully requested.

Rejections under 35 USC 112

Claims 1-3 stand rejected under 35 USC 112. These rejections are respectfully traversed.

Referring to Fig. 2 of the present invention, the output terminal 52 of the multiplexer 50 is coupled to the clock input terminal 32b of the circuit block 30b. When the circuit block 30b is configured to operate in synchronization with the circuit block 30a, the multiplexer 50 couples the source clock CLK1 to the clock input terminal 32b of the circuit block 30b, that is, the circuit block 30b receives the source clock CLK1 by the clock input terminal 32b. When the circuit block 30b operates asynchronously to the circuit block 30a, the multiplexer 50 couples the source clock CLK2 to the clock input terminal 32b of the circuit block 30b, that is, the circuit block 30b receives the source clock CLK2 by the clock input terminal 32b. Thus, the circuit block 30b receives the source clocks CLK1 and CLK2 by the same clock input terminal 32b.

According to claim 1, the clock input terminal (32b) of the second circuit block 30b receives the second source clock (CLK2).

When the second circuit block (30b) is configured to operate in synchronization with the first circuit block (30a), the clock input terminal (32b) of the second circuit block 30b is switched to receive the first source clock (CLK1). There is only one clock input terminal of the second circuit block for receiving the first or second source clocks.

Accordingly, it is respectfully submitted that claims 1-3 particularly point out and distinctly claim the subject matter of the instant invention. It is also respectfully submitted that claim 1 has not omitting an essential step, as it should be clear in the originally filed claim how the second circuit block is operated in accordance with the first source clock when switched. Reconsideration and withdrawal of the 35 USC 112, second paragraph rejections are respectfully requested.

Rejection under 35 USC 102(b)

Claims 1-3 stand rejected under 35 USC 102(b) as being anticipated by NAGAE, U.S. Patent 5,774,699. This rejection is respectfully traversed.

With regard to claim 1, it is respectfully submitted that NAGAE does not teach, disclose or suggest that a clock input terminal of a second circuit block is switched to a first source clock when the second circuit block is configured to operate in synchronization with a first circuit block.

Referring to Fig. 6 of NAGAE, the CPU receives the clock CPCLK0, and the selector 35 selects the clocks CPCLK0 or CPCLK1 to output to the CPU controller 29 according to the clock switching signal XTEST1. NAGAE does not teach that the selector 35 selects the clocks CPCLK0 in a predetermined operation mode, such as, a mode in which the CPU controller 29 is configured to operate in synchronization with the CPU.

However, according to the claimed invention, the circuit block 30a receives the source clock CLK1 and the multiplexer 50 selects the source clock CLK1 to output to the circuit block 30b when the circuit block 30b is configured to operate in synchronization with the circuit block 30a.

With regard to claim 1, it is respectfully submitted that NAGAE does not teach, disclose or suggest that an operation mode signal with a first state is set for the second circuit block operates in synchronization with a first circuit block.

According to NAGAE, when the clock switching signal XTESTI is "0", the selector 35 selects the clock CPCLK1, and when the clock switching signal XTESTI is "1", the selector 35 selects the clock CPCLK0. NAGAE does not teach that the clock switching signal XTESTI is "0" or "1" when the CPU controller 29 is configured to operate in synchronization with the CPU.

However, according to the claimed invention, the operation mode signal SEL is set a first state when the circuit block 30b is

configured to operate in synchronization with the circuit block 30a.

With regard to claim 3, it is respectfully submitted that NAGAE does not teach, disclose or suggest that a clock input terminal of a second circuit block is switched to a first source clock when the second circuit block o operates asynchronously to a first circuit block.

Referring to Fig. 6 of NAGAE, the CPU receives the clock CPCLK0, and the selector 35 selects the clocks CPCLK0 or CPCLK1 to output to the CPU controller 29 according to the clock switching signal XTEST1. NAGAE does not teach that the selector 35 selects the clocks CPCLK1 in a predetermined operation mode, such as, a mode in which the CPU controller 29 operates asynchronously to the CPU.

However, according to the claimed invention, the circuit block 30a receives the source clock CLK1 and the multiplexer 50 selects the source clock CLK0 to output to the circuit block 30b when the circuit block 30b operates asynchronously to the circuit block 30a.

Accordingly, in view of the foregoing amendments and remarks, it is respectfully submitted that the prior art utilized by the Examiner fails to teach or suggest the method set forth in independent claim 1 of the present application, as well as its dependent claims. Accordingly, reconsideration and withdrawal of the 35 USC 102(b) rejection are respectfully requested.

Allowable Subject Matter

Applicants gratefully acknowledge that the Examiner considers claims 4-7 to be allowable. In view of the foregoing amendments and remarks, it is respectfully submitted that all claims should be in condition for allowance.

Conclusion

Favorable reconsideration and an early Notice of Allowance are earnestly solicited.

In the event that any outstanding matters remain in this application, the Examiner is invited to contact the undersigned at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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